REMARKS

Claims 1-3 are pending in this application, of which claims 1-2 have been amended. No new claims have been added.

Claims 1-3 stand rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent 5,994,935 to Ueda et al. (hereinafter "**Ueda et al.**") in view of Nakata et al. ("A Low Power Multiplier Using Adiabatic Charging Binary Decision Diagram Circuit", Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pages 444-445 (hereinafter "**Nakata et al.**").

Applicants respectfully traverse this rejection.

Ueda et al. discloses a flip-flop circuit formed of two latch circuits of the same structure that are cascaded. The latch circuits include an inverter formed of a P channel transistor and an N channel transistor, an N channel transistor connected between a common node and a ground node, and two data input/output terminals. Two kinds of clock signals supplied to gates of N channel transistors are complementary to each other.

Fig. 2B shows clock signals CK and CKB 180° out of phase with each other.

The Examiner has admitted that **Ueda et al.** fails to disclose that a switched capacitor regenerator is cited to generate the clock signal, but has cited Fig. 4 of **Nakata et al.** for showing such a "switched capacitor regenerator".

Without admitting this, Applicants respectfully disagree with the Examiner's interpretation of the teachings of both **Ueda et al.** and **Nakata et al**.

Nakata et al. differs from the present invention in at least the following two ways:

(1) **Nakata et al.** relates to an adiabatic charging binary decision diagram (AC-BDD) multiplier, but not a register circuit, and

(2) **Nakata et al.** does not satisfy the claimed inequality. Indeed, **Nakata et al.** fails to teach, mention or suggest any relationship between a power source voltage (VDD), and the threshold voltages (V_{TN}, V_{TP}). It is not necessary in **Nakata et al.** to consider the inequality because it relates to an AC-BDD multiplier (not a register circuit), and an AC-BDD multiplier does not suffer from the problem of short circuit current (current flowing directly from a power source to ground), regardless of whether or not the inequality is satisfied.

Furthermore, the present invention combines a stepwise waveform clock signal with a first D-latch circuit and a second D-latch circuit in a particular manner, as recited in the claims, as amended.

Although the Examiner has urged that "any waveform generator could be used and the switched capacitor regenerator is one of them", Applicant respectfully disagrees. If a specific waveform generator provides a specific advantage, the combination of the specific waveform generator and a register circuit should be patentable over the prior art. The specific advantage in the current application is the decrease of power consumption in a register circuit.

Further, if a stepwise waveform clock signal were used in **Ueda et al.** and the inequality not satisfied, a short circuit current would flow from a power source (VDD) to a ground, because both a P-channel transistor and an N-channel transistor which is connected in series with said P-

channel transistor between a power source and a ground, conduct simultaneously. Therefore, the use of a stepwise waveform clock signal in the register circuit of **Ueda et al.** is essentially meaningless and not advantageous.

Thus, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-3, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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